Claim(s)

What is claimed is:

1. An apparatus responsive to input control data and commands for performing a test on a memory array having rows and columns of memory cells and for generating output data characterizing test results, wherein each memory cell resides in one row and in one column, wherein each row has a separate row address, wherein each column has a separate column address, and wherein each memory cell has a separate address formed by a unique combination of row and column addresses of the row and column in which the memory cell resides, the apparatus comprising:

a memory tester for testing each memory cell and producing fail data indicating whether the memory cell is defective; and

a plurality of counters, wherein each counter corresponds to an area of the memory array including only memory cells having addresses formed by any combination of row and column addresses within a particular row address range and a particular column address range separately specified for each counter by the input control data, and wherein each counter monitors the fail data produced by the memory tester to determine which memory cells are defective and generates a count of a number of defective memory cells residing within its corresponding area, such that counts produced by the counters characterize the test results.

2. The apparatus in accordance with claim 1 further comprising an error capture memory (ECM) having rows and columns of ECM cells, each for storing the fail data generated by the memory tester, wherein each ECM cell corresponds to a separate one of the memory cells, and wherein when the memory tester tests each memory cell, it sets the fail data in the memory cell's corresponding ECM cell to indicate whether the memory cell is defective.

3. The apparatus in accordance with claim 2, wherein the memory tester responds to a first input command

specifying a row address range and a column address range by reading the fail data in each ECM cell corresponding to memory cells residing within both the specified row and column address ranges.

4. The apparatus in accordance with claim 3 wherein when the memory tester reads fail data out of an ECM cell indicating that the corresponding memory cell is defective, the memory tester provides data identifying the defective memory cell as output data characterizing test results.

5. The apparatus in accordance with claim 4, wherein the memory tester responds to a second input command identifying one of either a row or a column of the memory array by reading the fail data in ECM cells corresponding to all memory cells of the identified row or column of the memory array, and signaling each counter to decrement its count when the fail data read out of any ECM cell corresponding to a memory cell within the counter's corresponding memory area indicates that the memory cell is defective.

6. The apparatus in accordance with claim 5 wherein the tester also responds to the second input command by setting the fail data stored in each ECM cell corresponding to a memory cell of the identified row or column identified by the second command to indicate that the corresponding memory cell is not defective.

7. A method for testing a memory array having addressable rows and columns of memory cells and for generating output data characterizing test results, wherein each memory cell has a separate address formed by a unique combination of row and column addresses of a row and a column in which the memory cell resides, the method comprising the steps of:

a. testing each memory cell to determine whether the memory cell is defective;

b. generating a separate count corresponding to each of a plurality of separately specified areas of the memory array, wherein each area encompassing only memory cells having addresses formed by any combination of row and column addresses lying with a range of row addresses and a range of column addresses, and

c. providing the counts as output data characterizing test results.

8. The method in accordance with claim 7 further comprising the steps of :

d. providing an error capture memory (ECM) having rows and columns of ECM cells for storing fail data, wherein each ECM cell corresponds to a separate one of the memory cells, and

e. setting the fail data in each ECM cell corresponding to a memory cell after the memory cell is tested at step (a) to indicate whether the corresponding memory cell is defective.

9. The method in accordance with claim 8, further comprising the step of:

f. responding to a first input command referencing an area corresponding to one of the counts by reading the fail data in each ECM cell corresponding to a memory cell residing within that area, and processing the fail data to generate output data characterizing test results by identifying each defective memory cell within the area specified by the first input command.

10. The method in accordance with claim 9 further comprising the step of:

g. responding to a second input command identifying one of either a row or a column of the memory array, by reading the fail data in ECM cells corresponding to all memory cells of the identified row or column, and

h. for each count, decrementing the count whenever the fail data read out of any ECM cell at step (g) indicates that

a memory cell within memory area corresponding to the count is defective.

11. The method in accordance with claim 10 further comprising the step of:

i. further responding to the second input command by setting the fail data stored in ECM cells corresponding to every memory cell of the row or column identified by the second input command to indicate that the corresponding memory cells are not defective.

12. A method for testing a random access memory (RAM) having addressable rows and columns of memory cells, and having spare rows and columns of memory cells, and for providing a computer with information enabling it to determine how to efficiently allocate spare rows and columns for replacing rows and columns containing defective memory cells, the method comprising the steps of:

a. testing each memory cell to determine whether it is defective;

b. writing fail data into an error capture memory (ECM) having ECM cells for storing fail data, wherein each ECM cell corresponds to a separate memory cell of the RAM, and wherein the fail data written into each ECM cell indicates whether its corresponding memory cell was determined at step (a) to be defective;

c. maintaining a plurality of counts, each count indicating a number of defective memory cells within a corresponding one of a plurality of separate areas of the RAM, wherein a particular set of memory cells included in each area is separately selected for each area by control data; and

d. providing the computer with access to the counts after all memory cells have been tested at step (a).

13. The method in accordance with claim 12 further comprising the steps of:

e. responding to a first input command from the computer identifying an area of the RAM corresponding to any one of the counts by reading out and processing fail data from ECM cells corresponding to memory cells included in the identified area;

f. processing the fail data read out at step (e) to generate results data indicating which memory cells within the identified area are defective; and

g. providing the results data to the computer.

14. The method in accordance with claim 13 further comprising the steps of:

h. responding to a second input command identifying one of either a row or a column of the RAM by reading the fail data in ECM cells corresponding to all memory cells of the identified row or column, and

i. for each count, decrementing the count whenever the fail data read out of any ECM cell at step (h) indicates that a memory cell within the memory area corresponding to the count is defective.

15. The apparatus in accordance with claim 14 further comprising the step of:

j. following step (h), further responding to the second input command to indicate that the corresponding memory cells are not defective.

16. An apparatus for performing a test on a memory array and generating data characterizing test results, wherein the memory array includes rows and columns of memory cells such that each memory cell resides in one row and in one column, wherein each row has a separate row address, wherein each column has a separate column address, and wherein each memory cell has an address formed by a unique combination of row and column addresses of the row and column in which the memory cell resides, the apparatus comprising:

a memory tester for testing each memory cell and producing fail data indicating whether the memory cell is defective; and

a plurality of counters,

wherein each counter corresponds to an area of the memory array,

wherein each counter monitors the fail data produced by the memory tester to determine which memory cells are defective and generates a count of a number of defective memory cells residing within its corresponding area, whereby counts produced by the counters characterize the test results, and

wherein a first counter of the plurality of counters corresponds to a first area of the memory array that is larger than, and wholly encompasses, a second area of the memory array to which a second counter corresponds.

17. The apparatus in accordance with claim 16 wherein the first area includes all of the memory array.

18. The apparatus in accordance with claim 17 wherein a third counter corresponds to a third area of the memory array, separate from the second area, smaller than the first area, and residing wholly within the first area.

19. The apparatus in accordance with claim 17 wherein a third counter corresponds to a third area of the memory array overlapping with the second area, smaller than the first area, and residing wholly within the first area.

20. An apparatus for performing a test on a memory array and generating data characterizing test results, wherein the memory array includes rows and columns of memory cells such that each memory cell resides in one row and in one column, wherein each row has a separate row address, wherein each column has a separate column address, and wherein each memory cell has an address formed by a unique

combination of row and column addresses of the row and column in which the memory cell resides, the apparatus comprising:

a memory tester for testing each memory cell and producing fail data indicating whether the memory cell is defective; and

a plurality of counters,

wherein each counter corresponds to an area of the memory array,

wherein each counter monitors the fail data produced by the memory tester to determine which memory cells are defective and generates a count of a number of defective memory cells residing within its corresponding area, whereby counts produced by the counters characterize the test results, and

wherein each of a first portion of counters of the plurality of counters corresponds to an area of the memory array encompassing all memory cells of a plurality of rows of the memory array, and

wherein each of a second portion of counters of the plurality of counters corresponds to an area of the memory array encompassing all memory cells of a plurality of columns of the memory array.

21. The apparatus in accordance with claim 20 wherein none of the areas to which the first portion of counters correspond overlap with one another, and

wherein none of the areas to which the second portion of counters correspond overlap with one another.

22. The apparatus in accordance with claim 21 further comprising an error capture memory (ECM) having rows and columns of ECM cells, each for storing the fail data generated by the memory tester, wherein each ECM cell corresponds to a separate one of the memory cells, and wherein when the memory tester tests each memory cell, it sets the fail data in the memory cell's corresponding ECM cell to indicate whether the memory cell is defective.